Chanyoung Moon

cmoon27@wisc.edu | rchan02@korea.ac.kr | moon-chanyoung.github.io | LinkedIn

RESEARCH INTERESTS

Computer Architecture, Hardware–Software Co-design, and Domain-Specific Accelerators

EDUCATION

University of Wisconsin–Madison *Sep. 2025 – May 2026*
Visiting Exchange Student, Electrical and Computer Engineering Madison, WI, USA

- GPA: 3.94/4.0

Korea University *Mar. 2021 – Aug. 2027 (Expected)*
B.E. in Electrical Engineering Seoul, South Korea

- Overall GPA: 4.44/4.5 (Upper-Division: 4.50/4.5), Major GPA: 4.46/4.5
- Leave of absence for mandatory military service: Apr. 2023 – Oct. 2024

PUBLICATIONS

[C.1] Chanyoung Moon, Travis Pence, Daisuke Yamada, Jiaqi Mo, Yanxin Zhang, Vikas Singh, Karthikeyan Sankaralingam. **FORGE: Procedural Weight Generation for Sparse MoE Inference** [paper]. ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2027).

[C.2] Travis Pence, Daisuke Yamada, Jiaqi Mo, Chanyoung Moon, Karthikeyan Sankaralingam, Vikas Singh. **Fast Sandwich Products in Clifford Algebra**. Advances in Neural Information Processing Systems (NeurIPS 2026).

[C.3] Chanyoung Moon, Hyung Jin Cho, Junil Kim, Seon Wook Kim. **Study for Behavior Verification and Resource Usage Analysis of RISC-V R-Type ISAs on FPGA**. IEIE Fall Conference 2022 (Korea).

RESEARCH EXPERIENCE

Vertical Research Group, University of Wisconsin–Madison *Oct. 2025 – Present*
Undergraduate Researcher (Advisor: Prof. Karthikeyan Sankaralingam) Madison, WI, USA

- **FORGE: Procedural Weight Generation for Sparse MoE Inference** (project lead; first author, **[C.1]**)
  - Designed the Rotor Generation Unit (RGU), an on-SM accelerator that regenerates MoE expert weights from compact seeds to remove HBM weight traffic, raising system throughput 1.3–2.8× and cutting parameter memory 28–29% at ∼0.9% GPU SM area (7 nm).
  - Exposed three axes of data parallelism in the generation algorithm and mapped them onto the RGU datapath; implemented and verified the RTL in SystemVerilog (cocotb, Verilator) and synthesized it for area and timing.
  - Built a system-level simulator to project end-to-end speedup; later integrated RGU into Accel-Sim (cycle-level).
- **Fast Sandwich Products in Clifford Algebra:** Contributed to the GPU kernel for the rotor sandwich product with bank-conflict-free shared-memory access, enabling larger rotor-based layers with up to 64× wall-clock and 35× memory improvements over prior implementations (**[C.2]**).
- **Closed-Loop Neural–Machine Interface System Simulation:** Leading a simulation-first BCI/exoskeleton co-design project; building its simulator, which models the sensorimotor loop as a multi-rate dependency graph under a sub-100 ms budget to identify architectural bottlenecks.
- **3D Gaussian Splatting Rendering Acceleration:** Profiled GEMM-GS (DAC 2026) on H100; showed naive INT8 tensor-core quantization collapses PSNR (25.5→17.3) for only 1.36×, and identified true inter-Gaussian dependencies in alpha blending as the fundamental limit to further parallelization.

Computer Systems Laboratory (CSL), Korea University *Sep. 2026 – Present*
Undergraduate Researcher, Senior Thesis (Advisor: Prof. Jeongseob Ahn) Seoul, South Korea

- Built a write-back, exclusive CPU-tier KV cache policy in vLLM to use scarce host DRAM efficiently in agentic LLM serving, raising throughput 21–30% over vLLM's default when the CPU tier is 0.8–1.6× the GPU KV pool; developed an analytical recompute model that predicts throughput within 2% across 46 runs (preliminary).

Compiler & Microarchitecture Lab (COMMIT), Korea University *Jul. 2022 – Sep. 2022*
Undergraduate Research Intern (Advisor: Prof. Seon Wook Kim) Seoul, South Korea

- Designed a modular RISC-V R-type core in Verilog and verified 13 instructions on a ZedBoard FPGA; characterized its footprint (589 LUTs, 263 registers) as a baseline for sizing ISA extensions; first-authored **[C.3]**.

HONORS AND AWARDS

Minister of Trade, Industry and Resources Award *Sep. 2026*
1st place among 213 scholars; Korean government award for outstanding academic and research achievement through the Korea–U.S. Advanced Fields Youth Exchange Program

NRF Undergraduate Research Fellowship (∼$4,500) *Sep. 2026 – Feb. 2027*
National Research Foundation of Korea (for outstanding STEM undergraduates pursuing research careers)

3rd Korea–U.S. Advanced Fields Youth Exchange Scholarship (∼$18,000) *2025 – 2026*
Ministry of Trade, Industry and Resources, Republic of Korea

Endowment Scholarship (∼$3,700, Awarded to Top Student) *May 2025*
School of Electrical Engineering, Korea University

Academic Excellence Scholarship (∼$11,200 total) *Spring 2022, Spring 2025, Fall 2025*
Korea University (awarded for 4.5/4.5 GPA)

Guwon Scholarship Foundation Award for Academic Excellence (∼$1,800) *2022*

Dean's Award, Korea University (4.5/4.5 semester GPA) *Fall 2021, Fall 2022, Spring 2025*

Semester Highest Honors, Korea University *5 semesters, 2021 – 2025*

LEADERSHIP & EXTRACURRICULAR ACTIVITIES

Architecture & System for AI Seminar, HandS, Korea University *Sep. 2026 – Present*

- Co-hosted a weekly seminar for 21 students; lectured on GPUs, HBM, interconnects, and LLM serving.

Korean Language Buddy, Korean Language Center, Korea University *Sep. 2026 – Present*

- Tutored two international students (English- and Japanese-speaking) in Korean weekly, totaling 50+ hours.

Study Abroad Program, Korea Foundation for Advanced Studies (KFAS) *Jun. 2026 – Present*

- One of 5 ECE students selected nationwide.

Young Engineers Honor Society (YEHS) *May 2025 – Present*

- Dean-recommended honor society of the National Academy of Engineering of Korea (NAEK).

Defense Communication Command, Republic of Korea Army *Apr. 2023 – Oct. 2024*
Microwave Communications Operator (Squad Leader) Daejeon, South Korea

- Led a 10-member squad; participated in two ROK–US combined forces exercises (UFS 2023, 2024).

Woonhwa Club, Korea University *Apr. 2021 – Aug. 2022*
Vice President, 53rd Cohort Seoul, South Korea

- Taught weekly science classes to 18 middle-schoolers from underserved households (144 hours).
- Raised $10,000+ in alumni sponsorship to fund the study room's rent and club operations.

SKILLS

- **Programming & Hardware Description:** C, C++, CUDA, Python, Verilog, SystemVerilog
- **EDA & Verification:** Synopsys DC, Yosys, Vivado, Quartus, ModelSim, cocotb, Verilator, Icarus Verilog
- **Performance Analysis & Simulation:** Accel-Sim, CACTI, NVIDIA Nsight Compute (NCU)